Analytical Method for Determining Equivalent Circuit Parameters of GaAs FET's

Shigeru Yanagawa, *Member, IEEE,* Hiroshi Ishihara, and Motoharu Ohtomo, *Senior Member, IEEE*

***Abstract*—An analytical method has been developed that gives a simple and practical means of extracting small-signal equivalent circuit parameters (ECP's) of GaAs FET's with negligibly small bond-pad capacitances. Only the S-parameter measurement of the pinched-off cold field-effect transistor (FET) is enough to determine the extrinsic FET ECP's. The intrinsic FET ECP's of a medium-power Ku-band GaAs FET chip with a total gate width of 800 μm have been analytically extracted for two types of eight-element intrinsic FET models; Model 1 (Curtice model) and Model 2 that differ in the control voltage (V_G) definition. Model 2 with V_G defined across the gate-source capacitance is found more appropriate judging from the smaller frequency dependence of the ECP's and a better agreement between the calculated and measured S-parameters over 2–20 GHz.**

I. Introduction

SMALL-SIGNAL equivalent circuit parameters (ECP's) of microwave field-effect transistor (FET's) are very useful for the performance evaluation and analysis of not only low-noise but also power devices. Various methods have been reported [1]–[7] for extracting ECP's, either intrinsic, extrinsic, or both from S-parameter measurements by using numerical optimization [1]–[3] or analytical methods [4]–[7]. Numerical optimization, however, may sometimes give rise to the local minimum problem depending upon the given initial values [1], [3] while the analytical method allows us to extract the ECP's straightforwardly. In order to deembed the intrinsic FET, the so-called cold-FET or the zero-drain-bias technique is widely used in various ways to determine the extrinsic ECP's. The cold-FET techniques reported so far, however, require S-parameter measurements on a cold FET under several forward-biased conditions [5], or pinched-off as well as forward-biased conditions [6].

Two types of equivalent circuit models are commonly used to represent an intrinsic FET; the seven-element model [2]–[6] and the eight-element model [1], [7], and [8]. Contrary to the eight-element model, the seven-element model cannot account for the observed positive reverse transfer conductance, i.e., Re $(y_{12} > 0)$ [1], [7] due to the lack of a drain-to-channel feedback capacitance. The eight-element model is further categorized into two, called Model 1 and Model 2. In Model 1, sometimes called the Curtice model [1], the control voltage V_G is defined across C_{GS} and R_I [1], [7], while in Model 2, V_G is defined across C_{GS} [8].

Manuscript received June 11, 1995; revised June 14, 1996.

S. Yanagawa and H. Ishihara are with Komukai Works, Toshiba Corporation, 1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan.

M. Ohtomo is with the Department of Electronics, Tokyo Engineering University, 1404-1, Katakura-cho, Hachioji 192, Japan.

Publisher Item Identifier S 0018-9480(96)06899-8.

The purpose of this paper is to propose a simple and practical analytical parameter extraction method for GaAs FET chips. Gate and drain bond-pad capacitances (C_{PG} and C_{PD}) are assumed to be negligibly small as compared to the input and output admittances of the intrinsic FET, which is often the case with medium-power GaAs FET's. It is shown that only S-parameter measurements on a pinched-off cold FET are enough to analytically extract extrinsic ECP's of the eight-element models. The intrinsic ECP's of a Ku-band medium power GaAs FET are analytically extracted and compared for both models.

II. Equivalent Circuits of Cold and Hot FET's

The equivalent circuit of a FET chip can be represented by Fig. 1(a), where L_G, L_D, and L_S represent the inductances of the gate, drain and source bond-wires, respectively, and C_{PG} and C_{PD} represent the gate and drain bond-pad capacitances, respectively. In our medium-power GaAs FET chip, C_{PG} and C_{PD} are estimated to be 0.012 pF and 0.011 pF, respectively, from the chip geometry to be mentioned later. R_G, R_D, and R_S represent the gate, drain, and source resistances, respectively.

Since R_G and R_D are of the order of 1 Ω, we have $\omega R_G C_{PG}$ and $\omega R_D C_{PD} \lesssim 10^{-3}$ for frequencies up to around 20 GHz, and without essential loss of accuracy we can transfer C_{PG} and C_{PD} to the right of R_G and to the left of R_D, respectively, as shown in Fig. 1(b). Then C_{PG} and C_{PD} can be neglected as shown in Fig. 1(c) if $|E_1| \ll 1$ and $|E^2| \ll 1$ hold (see the Appendix), where

$$E_1 = \frac{j\omega C_{PG}}{y_{11}} \frac{1 + Z_S \Sigma_y}{1 + \dfrac{Z_S \Delta_y}{y_{11}}}, \tag{1}$$

$$E_2 = \frac{j\omega C_{PD}}{y_{22}} \frac{1 + Z_S \Sigma_y}{1 + \dfrac{Z_S \Delta_y}{y_{22}}}, \tag{2}$$

$$Z_S = R_S + j\omega L_S, \tag{3}$$

$$\Sigma_y = y_{11} + y_{12} + y_{21} + y_{22}, \tag{4}$$

$$\Delta_y = y_{11} y_{22} - y_{12} y_{21} \tag{5}$$

and y_{ij}'s $(i = 1, 2; j = 1, 2)$ are the Y-parameters of the intrinsic FET. For our medium-power GaAs FET, $|E_1|$ and $|E_2|$ have been found to be less than 6% for 2–20 GHz. Thus the following analysis is based on the simplified equivalent circuit of Fig. 1(c).

The eight-element model of the hot-state intrinsic FET is shown in Fig. 2(a). Model 1 (Curtice model) and Model 2 refer

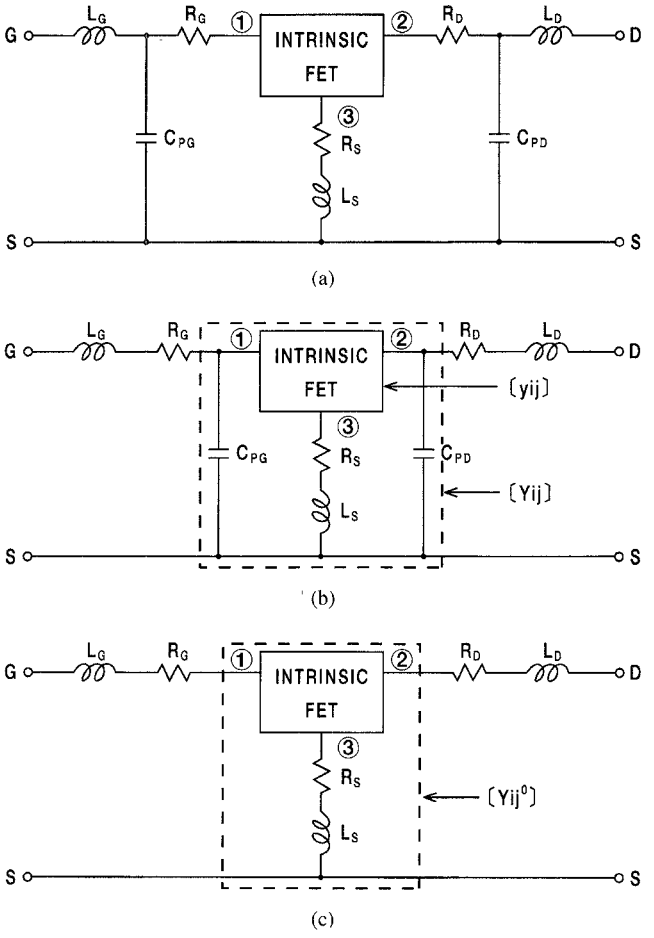

Fig. 1. (a) Equivalent circuit of FET chip mounted on microstrip test fixture, (b) equivalent circuit for $\omega R_G C_{PG} \ll 1$ and $\omega R_D C_{PD} \ll 1$, and (c) simplified equivalent circuit for negligibly small C_{PG} and C_{PD}.

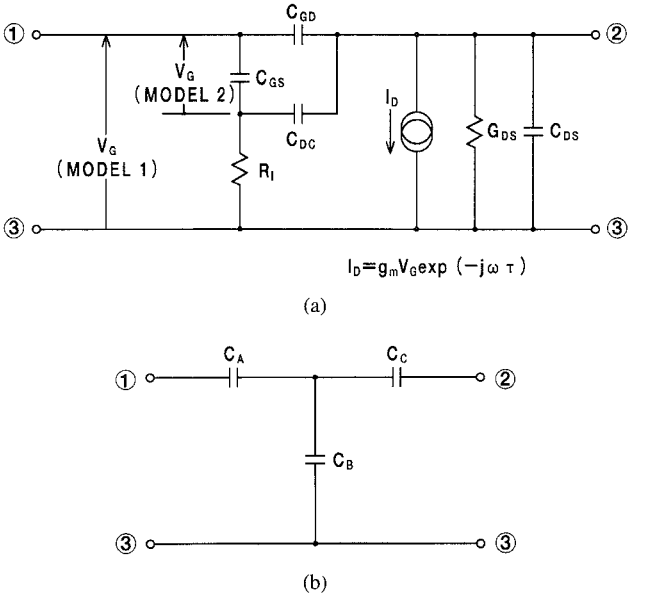

Fig. 2. Equivalent circuit for intrinsic FET, (a) hot FET (Model 1 and Model 2), and (b) pinched-off cold FET.

to the cases with the control voltage V_G that develops between $C_{GS}+R_I$ [1], [7] and C_{GS} [8], respectively. The equivalent circuit of the cold-state intrinsic FET can be represented by Fig. 2(b) by applying a $\Delta-Y$ transformation to the cold-FET equivalent circuit given in [3] and [6].

III. Analytical Extraction Method

The extrinsic ECP's in Fig. 1(c) can be analytically obtained from the S-parameter measurement on a pinched-off cold FET as in the following. Combining the equivalent circuits in Figs. 1(c) and 2(b), one obtains the Z-parameters (Z_{Cij}) of the pinched-off cold FET as

$$Z_{C11} = R_G + R_S + j\left\{\omega(L_G+L_S) - \frac{1}{\omega C_{AB}}\right\}, \quad (6)$$

$$Z_{C12} = Z_{C21} = R_S + j\left\{\omega L_S - \frac{1}{\omega C_B}\right\}, \quad (7)$$

$$Z_{C22} = R_D + R_S + j\left\{\omega(L_D+L_S) - \frac{1}{\omega C_{BC}}\right\} \quad (8)$$

where $C_{AB}^{-1} = C_A^{-1} + C_B^{-1}$ and $C_{BC}^{-1} = C_B^{-1} + C_C^{-1}$.

From (6)–(8), we then have

$$R_G = \mathrm{Re}\,(Z_{C11} - Z_{C12}), \quad (9)$$

$$R_S = \mathrm{Re}\,(Z_{C12}) = \mathrm{Re}\,(Z_{C21}), \quad (10)$$

$$R_D = \mathrm{Re}\,(Z_{C22} - Z_{C12}), \quad (11)$$

$$\omega\,\mathrm{Im}\,(Z_{C11}) = \omega^2(L_G+L_S) - \frac{1}{C_{AB}}, \quad (12)$$

$$\omega\,\mathrm{Im}\,(Z_{C12}) = \omega^2 L_S - \frac{1}{C_B}, \quad (13)$$

$$\omega\,\mathrm{Im}\,(Z_{C22}) = \omega^2(L_D+L_S) - \frac{1}{C_{BC}}. \quad (14)$$

Equations (9)–(11) mean that the values of R_G, R_S, and R_D are readily determined at each frequency of measurement by the Z_{Cij}'s converted from the measured S-parameters of the cold FET. Meanwhile (12)–(14) indicate that, if we plot $\omega\,\mathrm{Im}\,(Z_{C11})$ $\omega\,\mathrm{Im}\,(Z_{C12})$, and $\omega\,\mathrm{Im}\,(Z_{C22})$ against ω^2, each plot should be on a straight line with a slope equal to L_G+L_S, L_S, or L_D+L_S. From these slopes we can readily obtain the values of L_G, L_S, and L_D.

After determining the extrinsic parameters in this way, the Y-parameters of the intrinsic hot FET, y_{ij} can be obtained by deembedding from the measured S-parameters using matrix manipulations as given in [4]. If the equivalent circuit parameters of the intrinsic FET are analytically expressed by the y_{ij}'s, their values can be determined straightforwardly.

For both Model 1 and Model 2, the relations of C_{GS}, C_{DC}, C_{GD}, and R_I with y_{ij}'s are the same and given by

$$C_{GS} = \frac{|y_{11}+y_{12}|^2}{\omega\,\mathrm{Im}\,(y_{11}+y_{12})}, \quad (15)$$

$$C_{DC} = \frac{C_{GS}\,\mathrm{Re}\,(y_{12})}{\mathrm{Re}\,(y_{11})}, \quad (16)$$

$$C_{GD} = -\frac{\mathrm{Im}\,(y_{12})}{\omega} - \frac{\omega^2\tau_1\tau_2 C_{GS}}{1+(\omega\tau_2)^2}, \quad (17)$$

$$R_I = \frac{\mathrm{Re}\,(y_{11})}{\omega C_{GS}\,\mathrm{Im}\,(y_{11}+y_{12})} \quad (18)$$

where

$$\tau_1 = R_I C_{DC}, \tag{19}$$

$$\tau_2 = R_I(C_{GS} + C_{DC}). \tag{20}$$

For Model 1, g_m, τ, G_{DS}, and C_{DS} are given by

$$g_m = |y_{21} - y_{12}|, \tag{21a}$$

$$\tau = -\frac{1}{\omega}\tan^{-1}\left\{\frac{\mathrm{Im}\,(y_{12} - y_{21})}{\mathrm{Re}\,(y_{12} - y_{21})}\right\}, \tag{21b}$$

$$G_{DS} = \mathrm{Re}\,(y_{22}) - \frac{\omega^2\tau_1 C_{DC}}{1 + (\omega\tau_2)^2}, \tag{21c}$$

$$C_{DS} = \frac{\mathrm{Im}\,(y_{22})}{\omega} - C_{GD} - C_{DC}\left[1 - \frac{\omega^2\tau_1\tau_2}{1 + (\omega\tau_2)^2}\right]. \tag{21d}$$

These expressions are the same as those given in [7], except for (21a) and (21c) wherein low-frequency approximation is not employed. For Model 2, g_m, τ, G_{DS}, and C_{DS} are given by (22a)–(22d) as shown at the bottom of the page.

IV. Measurement of Equivalent Circuit Parameters

ECP's of a Ku-band 0.25 W power GaAs FET chip have been extracted using the method described in the previous section. The FET chip has a size of 370 × 480 μm with a thickness of 100 μm, a gate length of 0.5 μm, and a total gate width of 800 μm. The areas of the gate and drain bondpads are 8,200 μm^2 and 10 600 μm^2, respectively. The FET chip are mounted on a 50-Ω microstrip chip carrier with 250-μm thick alumina substrate. The gate and drain pads were bonded to the microstrip lines with a single gold wire of 25 μm diameter, while the source was grounded with six gold wires. S-parameter measurements have been performed over 2–20 GHz (2 GHz step) using an adjustable test fixture (Inter-Continental Microwave, Model TF-2001-K) and a TRL (thru-reflect-line) calibration kit (Inter-Continental Microwave, Model TRL-10-200).

In the cold FET measurement, the FET chip was biased at $V_{DS} = 10$ V and $V_{GS} = -5$ V well below pinch-off. After conversion of the measured S-parameters, $\omega\,\mathrm{Im}\,(Z_{C11})$, $\omega\,\mathrm{Im}\,(Z_{C12})$, and $\omega\,\mathrm{Im}\,(Z_{C22})$ are plotted against ω^2 as shown in Fig. 3, where straight lines obtained by the least-square curve fitting are also shown. It can be seen that the measured plots are fairly well on the straight lines. From the slopes of the straight lines, the values of L_G, L_S, and L_D have been determined to be 0.259 nH, 0.009 nH, and 0.291 nH, respectively. The values of R_G, R_S, and R_D have been calculated from (9)–(11) at each frequency of measurement. The average ± standard deviation has been found to be $0.89 \pm 0.15\,\Omega$, $0.27 \pm 0.08\,\Omega$, and $1.08 \pm 0.11\,\Omega$ for R_G, R_S, and R_D, respectively, over 2–20 GHz.

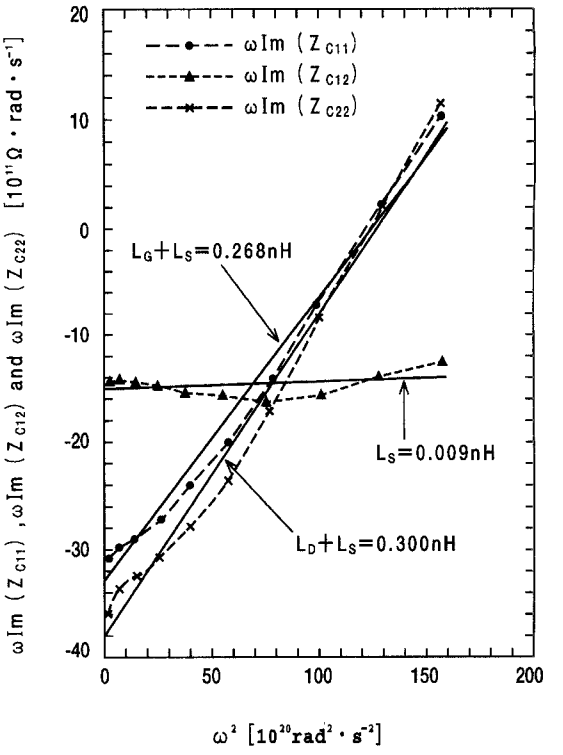

Fig. 3. Measured $\omega\,\mathrm{Im}\,(Z_{C_{ij}})$ against ω^2 for pinched-off cold FET for 2–20 GHz(2 GHz step).

The S-parameters have also been measured on a hot FET biased at typical operating bias conditions of $V_{DS} = 10$ V and $I_{DS} = 120$ mA ($\approx I_{DSS}/2$). The plots of measured S-parameters are shown in Fig. 4. The eight-element intrinsic ECP's of the hot FET are analytically determined from (15)–(21) for Model 1 and from (15)–(20) and (22) for Model 2. They are shown against frequency in Fig. 5. The average ± standard deviation of the intrinsic ECP's are also shown as the insets to Fig. 5. As mentioned in Section III, the values of C_{GS}, C_{DC}, C_{GD}, and R_I are the same for both models. C_{DS} and g_m are seen to be nearly independent of the models, while τ and G_{DS} are model dependent. The value of τ for Model 1 is about 50% larger than that for Model 2, being consistent

$$g_m = |y_{21} - y_{12}|\frac{\sqrt{1 + (\omega\tau_2)^2}}{\sqrt{1 + (\omega\tau_1)^2}}, \tag{22a}$$

$$\tau = \frac{1}{\omega}\left[-\tan^{-1}\left\{\frac{\mathrm{Im}\,(y_{12} - y_{21})}{\mathrm{Re}\,(y_{12} - y_{21})}\right\} + \tan^{-1}\left\{\frac{\omega(\tau_1 - \tau_2)}{1 + \omega^2\tau_1\tau_2}\right\}\right] \tag{22b}$$

$$G_{DS} = \mathrm{Re}\,(y_{22} + y_{21}) - \frac{g_m(\cos\omega\tau - \omega\tau_2\sin\omega\tau) + \omega^2\tau_1(C_{DC} + C_{GS})}{1 + (\omega\tau_2)^2} \tag{22c}$$

$$C_{DS} = \frac{\omega\tau_2\,\mathrm{Re}\,(y_{22} + y_{21}) + \mathrm{Im}\,(y_{22} + y_{21}) - \omega\tau_2 G_{DS} + g_m\sin\omega\tau}{\omega} - C_{DC} \tag{22d}$$

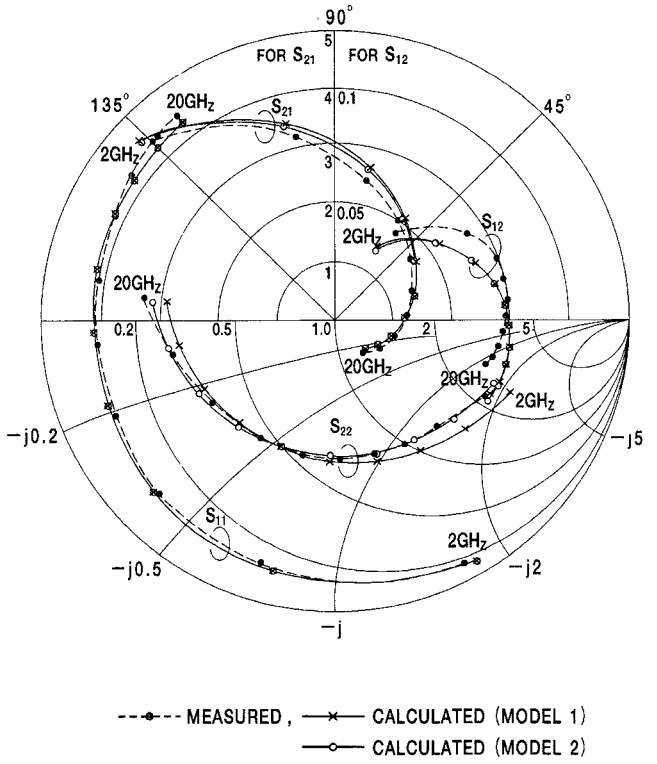

Fig. 4. Measured and calculated S-parameters of hot FET for 2–20 GHz at 2 GHz step (V_{DS} = 10 V, I_{DS} = 120 mA).

with the fact that Model 1 forces τ to account for all delay effects under the gate [1].

While G_{DS} is almost frequency independent for Model 2, it decreases almost linearly with frequency for Model 1 and its value at 20 GHz becomes nearly half of that at 2 GHz. This suggests that Model 2 is physically more appropriate than Model 1 (Curtice model) as far as the lumped-constant eight-element model is concerned. Considering that G_{DS} is an important parameter affecting the output impedance level of power GaAs FET's, it is suggested that Model 2 should be used to determine small-signal value of G_{DS}.

The S-parameters of the hot FET have been calculated using the analytically extracted ECP's and are plotted in Fig. 4 together with the measured ones for comparison, showing a generally good agreement between the calculation and the measurement. So far as S_{11}, S_{21}, and S_{12} are concerned, there can be seen essentially no difference between the calculations for Model 1 and Model 2. The calculated S_{22} for Model 2, however, agrees much better with the measurement than for Model 1.

The present analytical extraction method is based on the equivalent circuit shown in Fig. 1(c), i.e., C_{PG} and C_{PD} are assumed to be negligibly small. For our FET chip, C_{PG} is estimated to be 0.012 pF by adding the air-bridge capacitance of $\approx$0.0035 pF to the geometrical bond-pad capacitance. C_{PD} is calculated to be 0.011 pF. With the estimated values of C_{PG} and C_{PD}, the relative errors, E_1 and E_2 for neglecting C_{PG} and C_{PD} have been calculated using the measured S-parameters. It has been found that $|E_1|$ and $|E_2|$ are less than 4% in the case of cold FET, and less than 5.5% in the case of hot FET for 2–20 GHz.

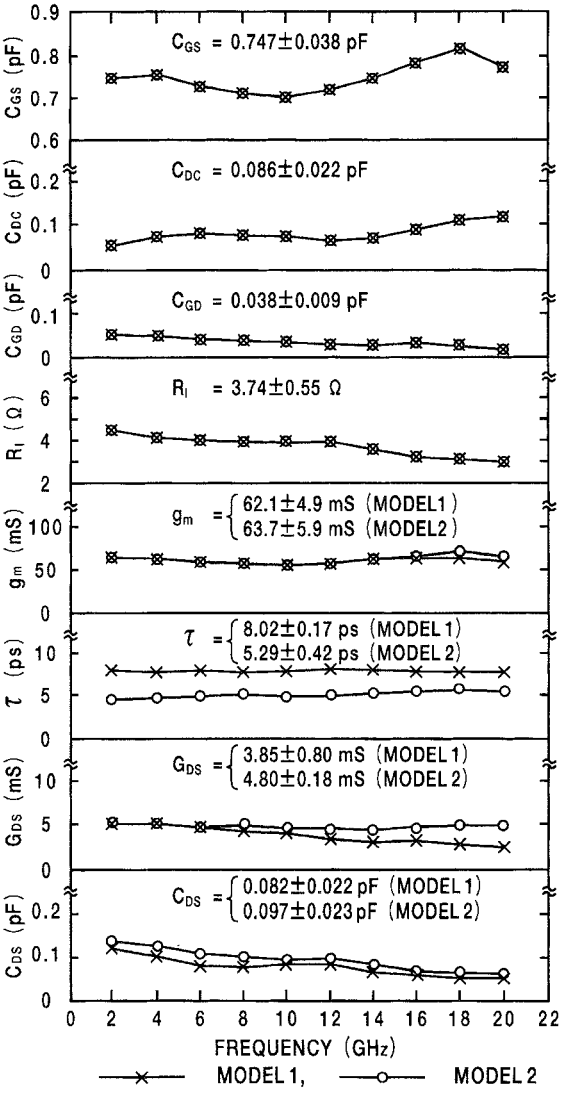

Fig. 5. Analytically extracted intrinsic ECP's for Model 1 and Model 2. Insets show average ± standard deviation over 2–20 GHz.

V. Conclusion

A method of analytically extracting small-signal ECP's of GaAs FET chips has been proposed. Only the S-parameter measurements of the pinched-off cold FET and normally-biased hot FET are enough to determine extrinsic and intrinsic ECP's. The method has been successfully applied to extract ECP's of a medium-power GaAs FET chip for 2–20 GHz, demonstrating that, among the two kinds of intrinsic hot FET models (Models 1 and 2), Model 2 gives less frequency-dependent values of ECP's and show a better agreement with the measured S-parameters. Though the method is based on a simplified equivalent circuit model, it gives a simple yet practical means of extracting ECP's of power GaAs FET's.

Appendix

Let us denote the Y-parameters of the dashed-line encircled twoport in Fig. 1(b) as Y_{ij}. Then we can obtain the following

relations between Y_{ij} and y_{ij}:

$$Y_{11} = y_{11}\frac{\left(1+\frac{Z_s\Delta_y}{y_{11}}\right)}{1+Z_s\Sigma_y} + j\omega C_{PG}$$
$$= \left\{ y_{11}\frac{\left(1+\frac{Z_s\Delta_y}{y_{11}}\right)}{1+Z_s\Sigma_y} \right\}(1+E_1),$$
$$Y_{12} = y_{12}\frac{\left(1-\frac{Z_s\Delta_y}{y_{12}}\right)}{1+Z_s\Sigma_y},$$
$$Y_{21} = y_{21}\frac{\left(1-\frac{Z_s\Delta_y}{y_{21}}\right)}{1+Z_s\Sigma_y},$$
$$Y_{22} = y_{22}\frac{\left(1+\frac{Z_s\Delta_y}{y_{22}}\right)}{1+Z_s\Sigma_y} + j\omega C_{PD}$$
$$= \left\{ y_{22}\frac{\left(1+\frac{Z_s\Delta_y}{y_{22}}\right)}{1+Z_s\Sigma_y} \right\}(1+E_2)$$

where E_1, E_2, Z_S, $\sum_y$, and Δ_y are defined by (1)–(5), respectively. Denoting Y_{ij} for the case of $C_{PG} = C_{PD} = 0$ as Y_{ij}^0, we then have

$$\frac{Y_{11}}{Y_{11}^0} = 1 + E_1,$$
$$\frac{Y_{12}}{Y_{12}^0} = \frac{Y_{21}}{Y_{21}^0} = 1,$$

and

$$\frac{Y_{22}}{Y_{22}^0} = 1 + E_2.$$

These expressions mean that the relative errors of Y_{11} and Y_{22} in neglecting C_{PG} and C_{PD} are E_1 and E_2,, respectively. If $|E_1|$ and $|E_2| \ll 1$, the relative errors of y_{11} and y_{22} are also nearly equal to E_1 and E_2,, respectively.

ACKNOWLEDGMENT

The authors wish to thank S. Watanabe for helpful comments and K. Kamei for his encouragement.

REFERENCES

[1] W. R. Curtice and R. L. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, no. 12, pp. 1573–1578, Dec. 1984.

[2] S. Bandla, G. Dawe, C. Bedard, R. Tayrani, D. Shaw, L. Raffaelli, and R. Goldwasser, "A 35 GHz monolithic MESFET LNA," in *IEEE MTT-S Dig.*, 1988, pp. 259–263.

[3] G. Kompa and M. Novotny, "Highly consistent FET model parameter extraction based on broadband S-parameter measurements," in *IEEE MTT-S Dig.*, 1992, pp. 293–296.

[4] G. Dambrine, A. Cappy, F. Heliodone, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, July 1988.

[5] R. Anholt and S. Swirhun, "Equivalent-circuit parameter extraction for cold GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 7, pp. 1243–1247, July, 1991.

[6] H. Sledzik and I. Wolff, "A new approach to nonlinear modeling and simulation of MESFET's and MODFET's," in *Proc. 20th Euro. Microwave Conf.*, 1990, pp. 784–789.

[7] H. O. Vickes, "Determination of intrinsic FET parameters using circuit partitioning approach," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 2, pp. 363–366, Feb. 1991.

[8] S. Akhtar and S. Tiwari "Non-quasi-static transient and small-signal two-dimensional modeling of GaAs MESFET's with emphasis on distributed effects," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2154–2163, Dec. 1993.

Shigeru Yanagawa (M'89) was born in Tokyo, Japan, on October 30, 1948. He received the B.E. degree in electrical engineering from Waseda University, Japan in 1971.

He joined Toshiba Corporation, Kawasaki, Japan, in 1971. From 1971 to 1978, he was engaged in research and development of TRAPATT and IMPATT oscillators at Toshiba Research and Development Center. He has been working on development of power GaAs FET's from 1979 at Toshiba Komukai Works. His current interests are nonlinear analysis of microwave and millimeter-wave devices.

Mr. Yanagawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.

Hiroshi Ishihara was born in Aichi, Japan, on July 22, 1962. He received the B.E. degree in electronics from Chiba Institute of Technology, Japan in 1985.

He joined Toshiba Corporation, Kawasaki, Japan, in 1985. From 1985 to 1988, he was engaged in development of low-noise GaAs FET's at Toshiba Komukai Works. Since 1989, he has been working on power GaAs FET's and HEMT's.

Motoharu Ohtomo (M'91–SM'94) was born in Osaka, Japan, on February 11, 1938. He received the B.E. degree in applied physics from the University of Tokyo, Japan in 1960, and the Dr. Eng. degree from the same university in 1976.

In 1960, he joined Toshiba Corporation, Kawasaki, Japan. From 1960 to 1979, he was engaged in research and development of microwave devices and components such as ruby masers, Gunn-effect devices, IMPATT and TRAPATT oscillators, MIC modules at Toshiba Research and Development Center. From 1979 to 1994, he was mainly engaged in R&D management of microwave semiconductor devices and components at Toshiba Komukai Works. In 1994, he left Toshiba and joined Tokyo Engineering University, Hachioji, Tokyo, Japan as a Professor at the Department of Electronics.

Dr. Ohtomo is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.